Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology

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Key Messages

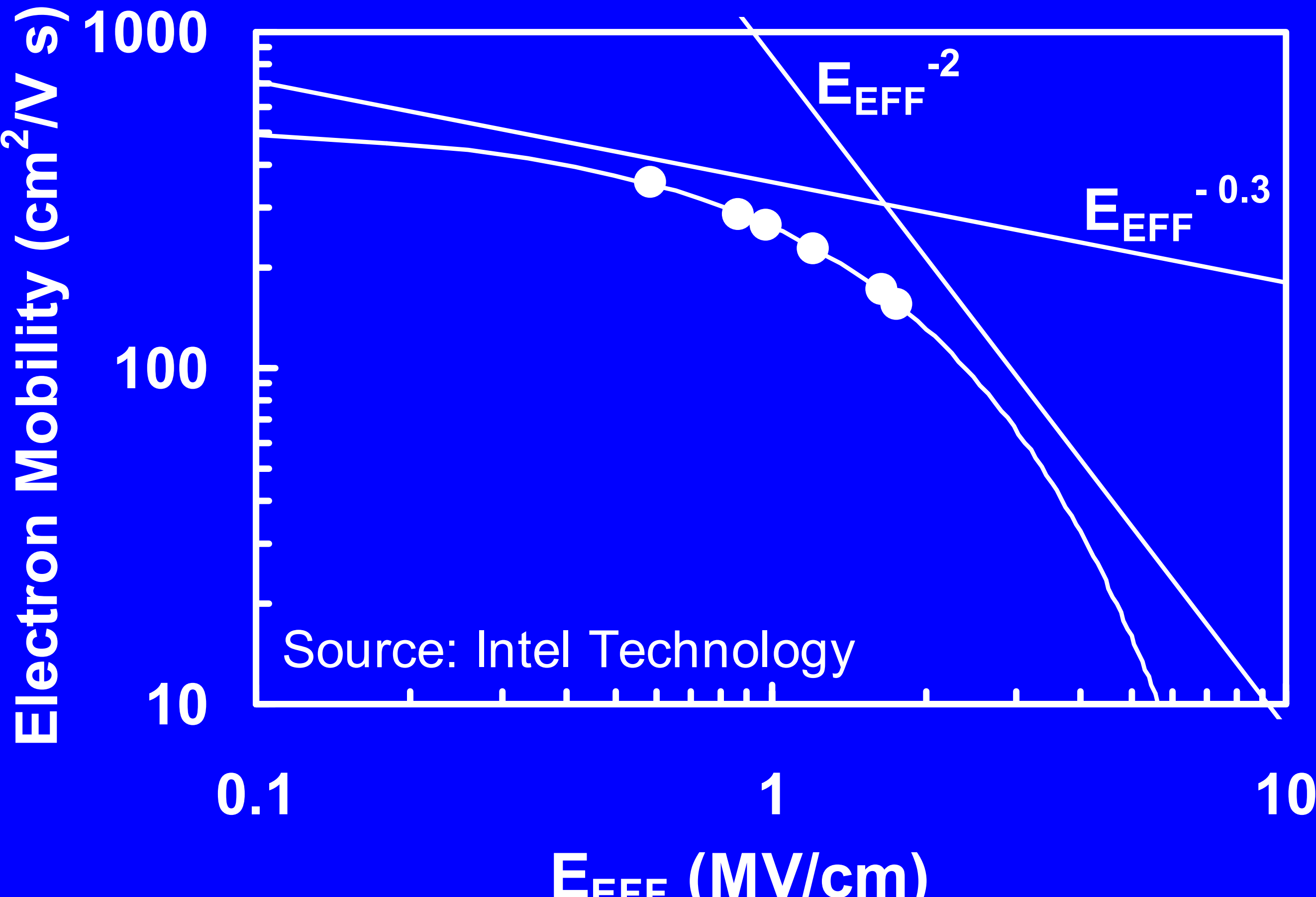
- Biaxial vs. Uniaxial strain
  - Electron mobility gain similar for both stress types
  - Hole mobility gain superior for uniaxial strain
- Epitaxial S/D transistor structure
  - Large uniaxial strain
  - Improved R_{EXT} so full mobility benefit is realized
- This is a high volume manufacturing technology

Outline

- Introduction
- Why Uniaxial Strain?
- Transistor Results
- Performance & Power
- Summary

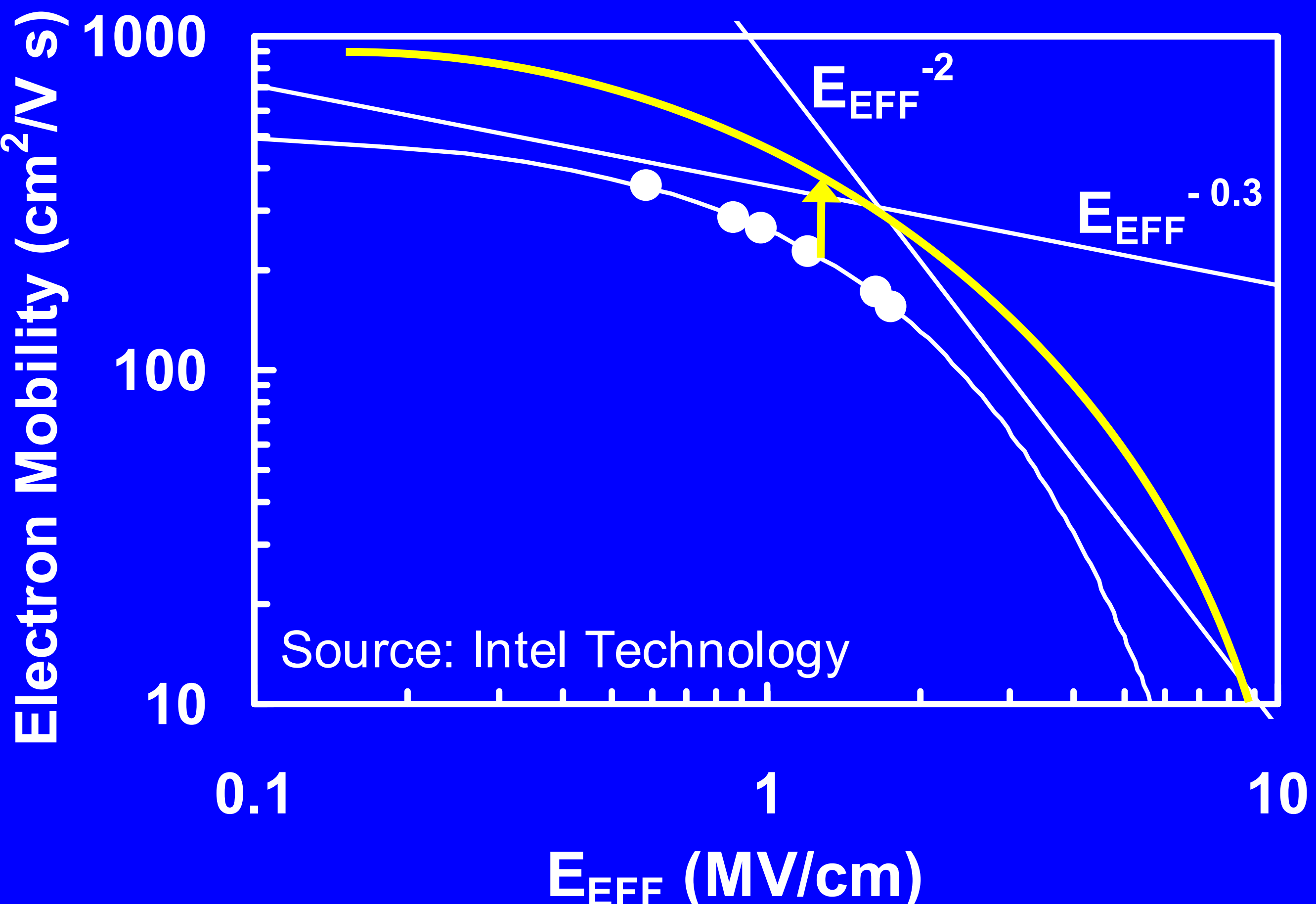
Transistor Scaling: The Mobility Challenge

- **Mobility degrades with transistor scaling**
  - Universal mobility model
  - Ionized impurity scattering



Strain Enhanced Mobility

- **Strain can be used to enhance mobility**
  - **Effect known for >50 years** [C.S. Smith, *Phys Rev*, 1954]



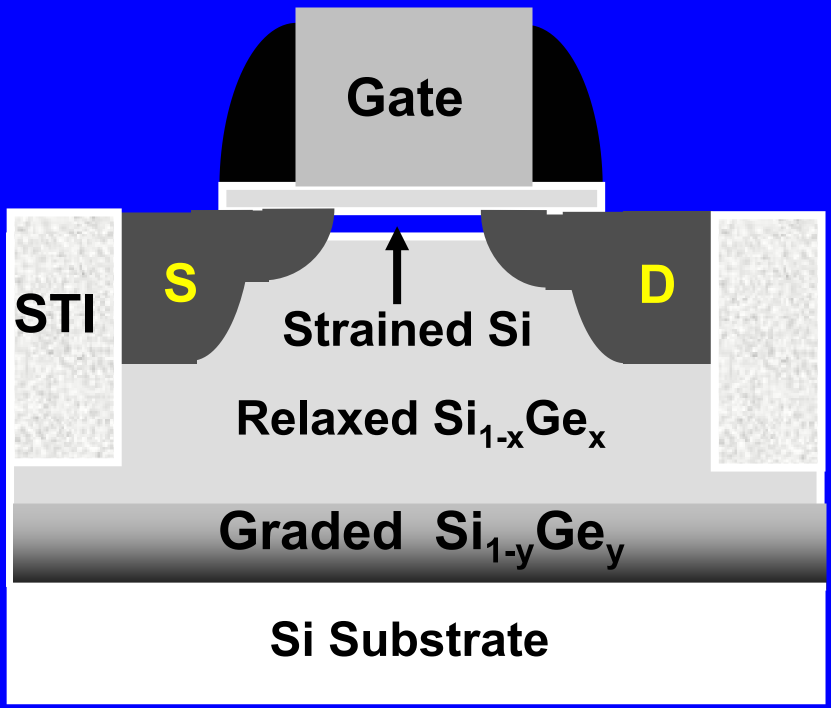
Biaxial Tensile Strain

Biaxial tensile strain studied extensively last 10 years

- Large electron mobility gain, but...

Two key problems:

1. Integration difficulties
   - Dislocations
   - Ge Up-diffusion
   - Fast diffusion of extensions
   - Cost
2. Poor hole mobility gain



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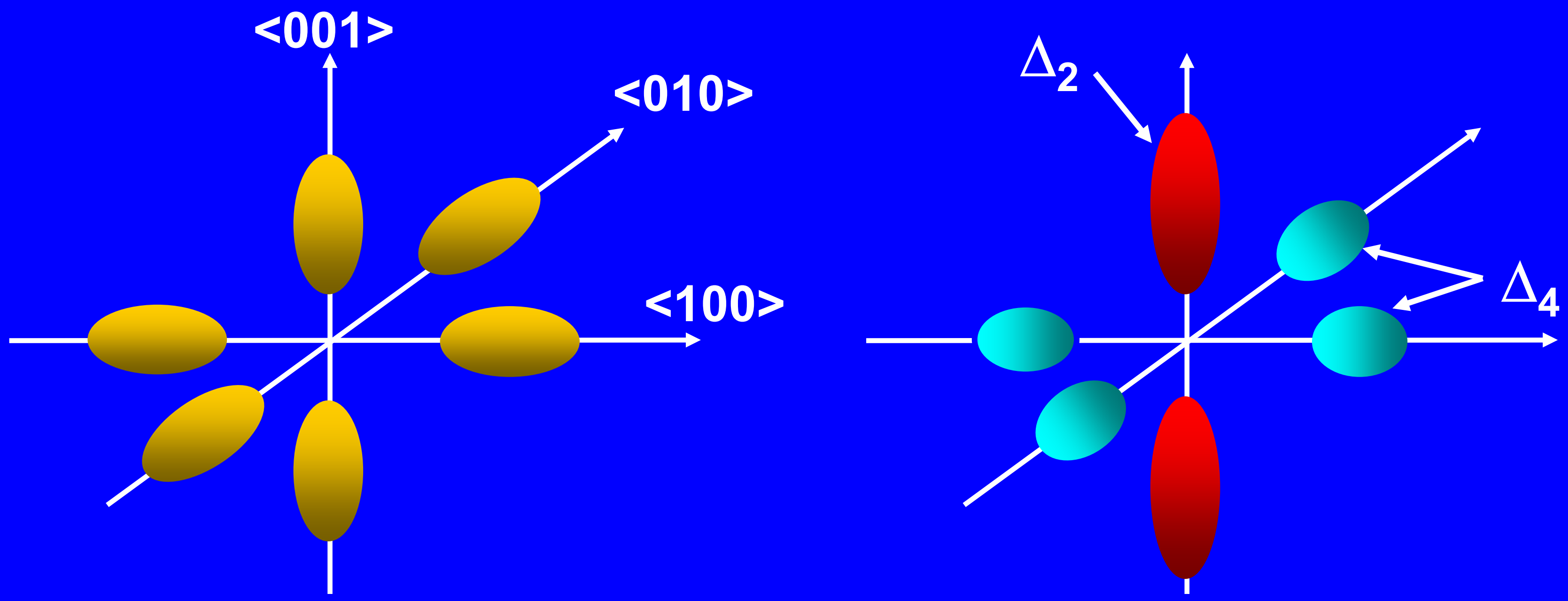
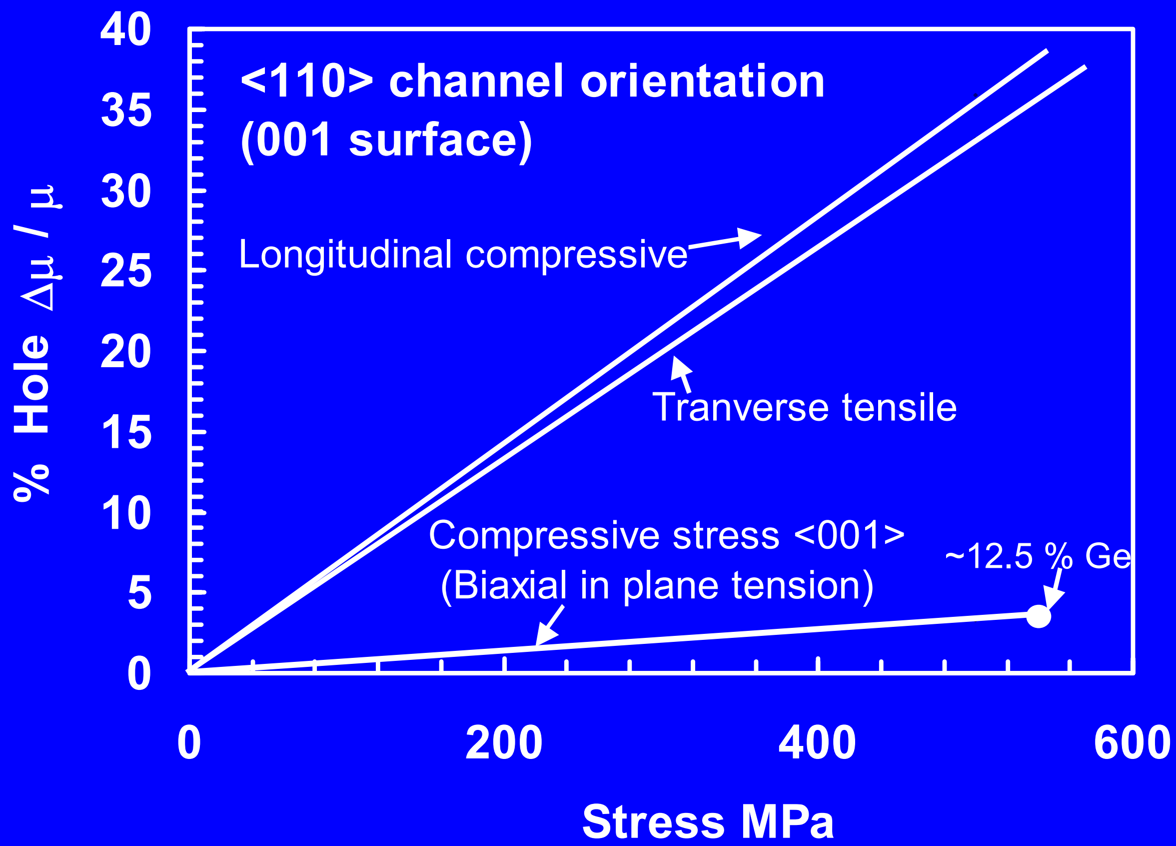
Biaxial vs. Uniaxial Strain: Electrons

- **Electron mobility enhancement similar**
  - Both cases result from splitting of 6-fold degenerate valleys
  - Only valley shifting responsible for mobility gain
  - Negligible band curvature change in either case



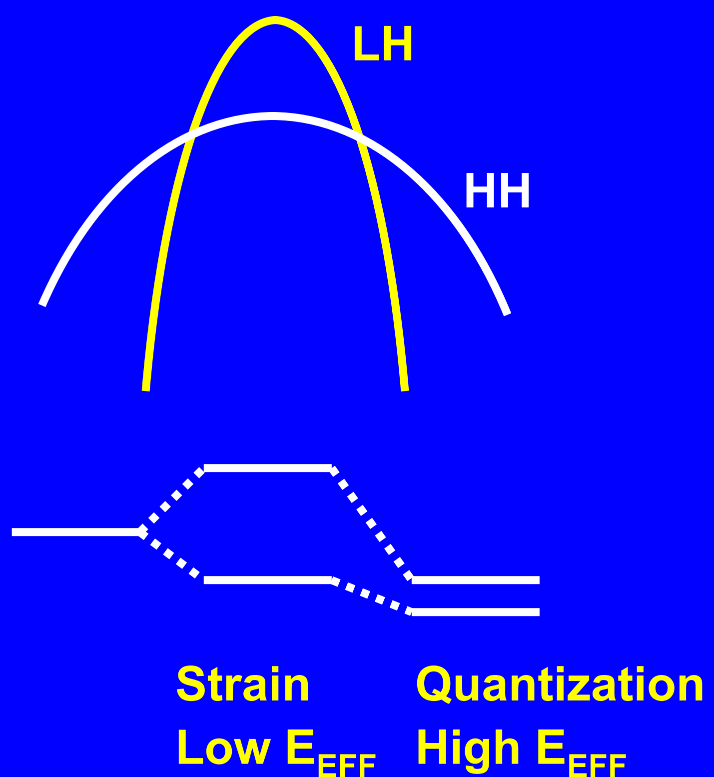
Biaxial vs. Uniaxial Strain: Holes

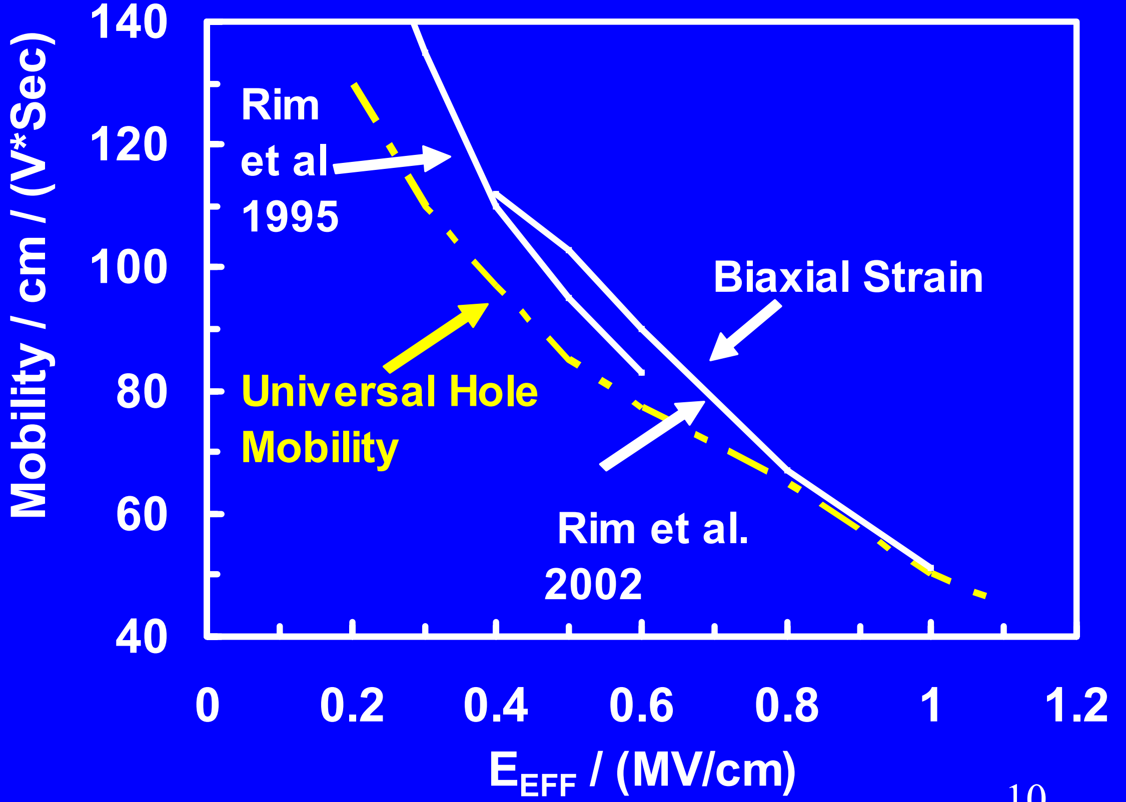
- **Uniaxial stress more effective than biaxial for hole mobility improvement**
  - **Simple calculations using peizoresistance coefficients** [C.S. Smith, *Phys. Rev.*, 1954]



Biaxial vs. Uniaxial Strain: Holes

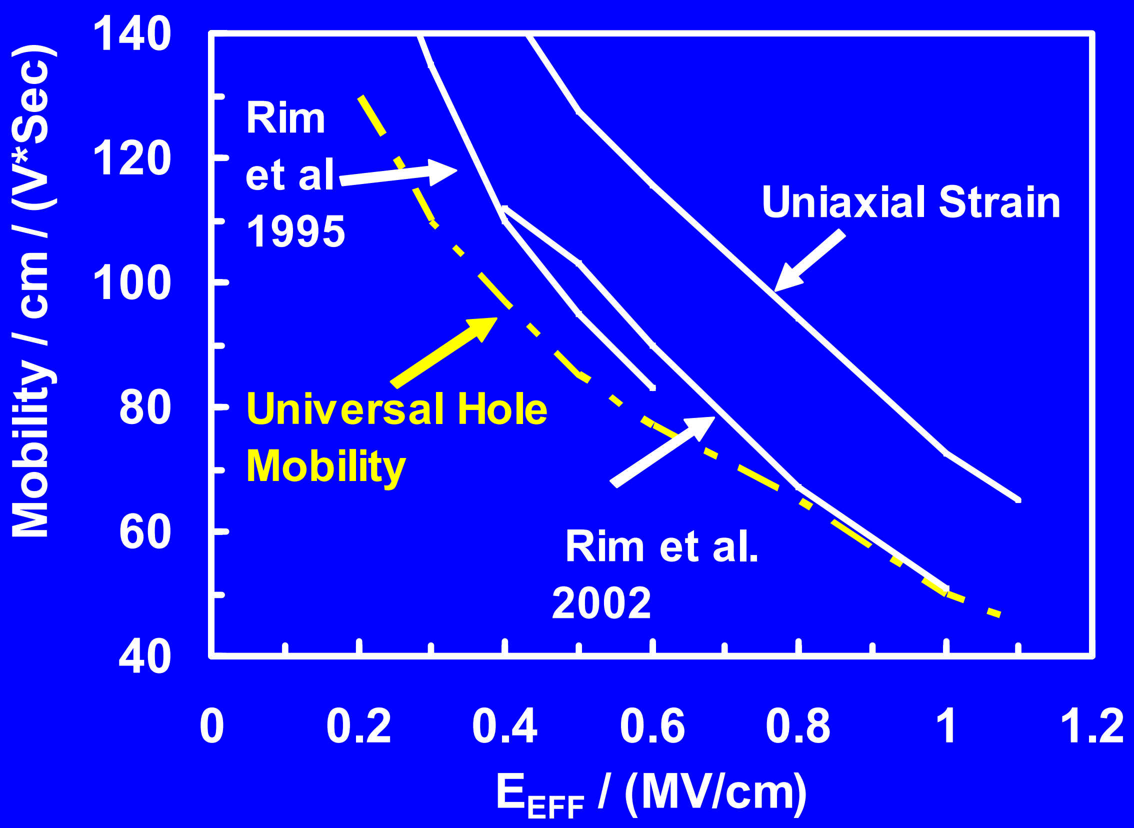
- **Biaxial strain: hole mobility gain lost at high E_{EFF}**
  - Mobility gain due to lower scattering: separation of LH & HH bands
    - ➔ Not due to reduction in hole effective mass
  - At high E_{EFF} LH – HH separation reduced due to quantization
    - ➔ Hole mobility gain is lost





Biaxial vs. Uniaxial Strain: Holes

- Uniaxial strain: high hole mobility at high E_{EFF}
  - Mobility gain from effective mass reduction
    - ➔ Change in band warping [Giles, VLSI04]
  - Band separation not reduced at high E_{EFF}
    - ➔ High out of plane effective mass for light holes



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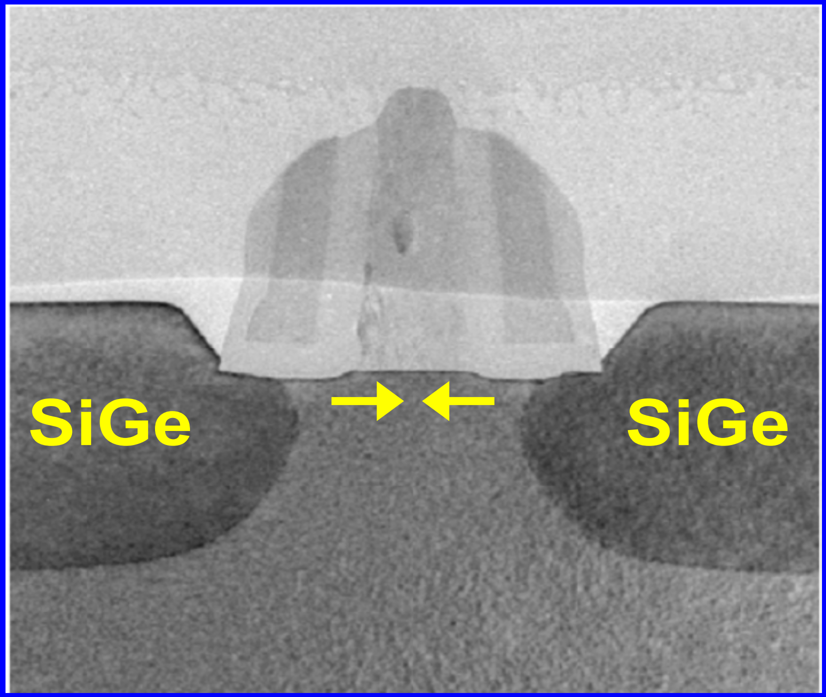
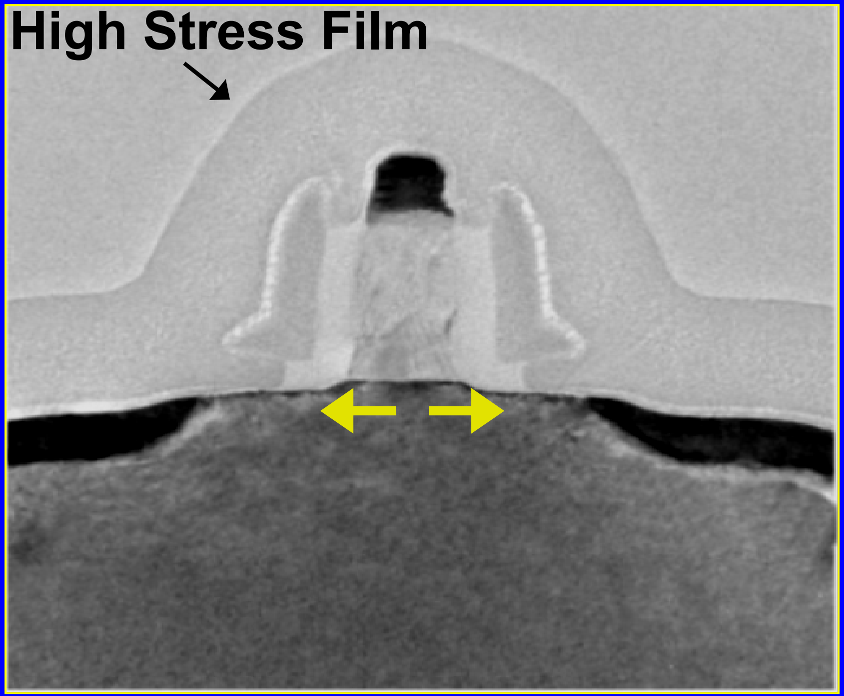
Uniaxial Strain Structures

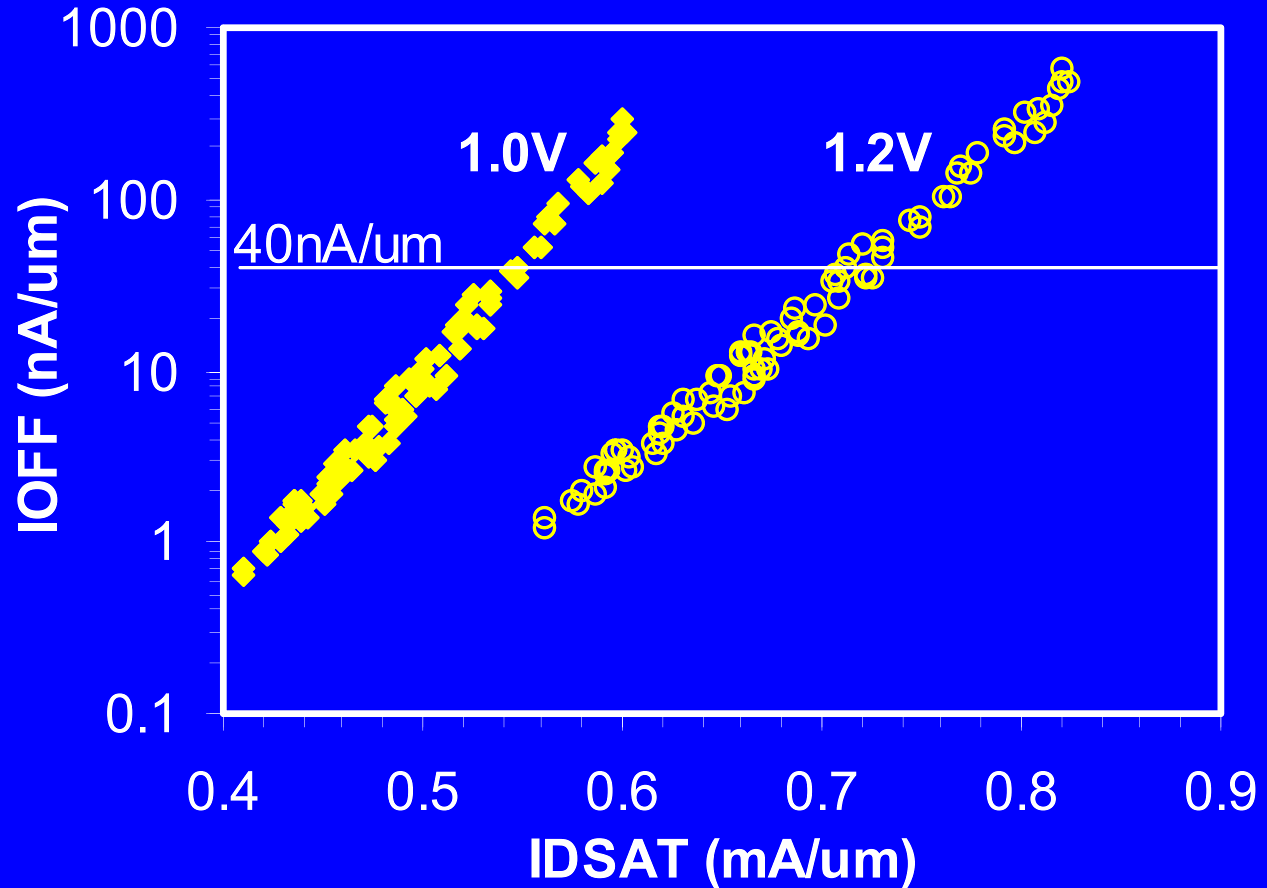
- Two uniaxial strain structures incorporated in our 90nm CMOS technology
  - Epitaxial S/D Transistor for PMOS
  - Tensile capping layer for NMOS





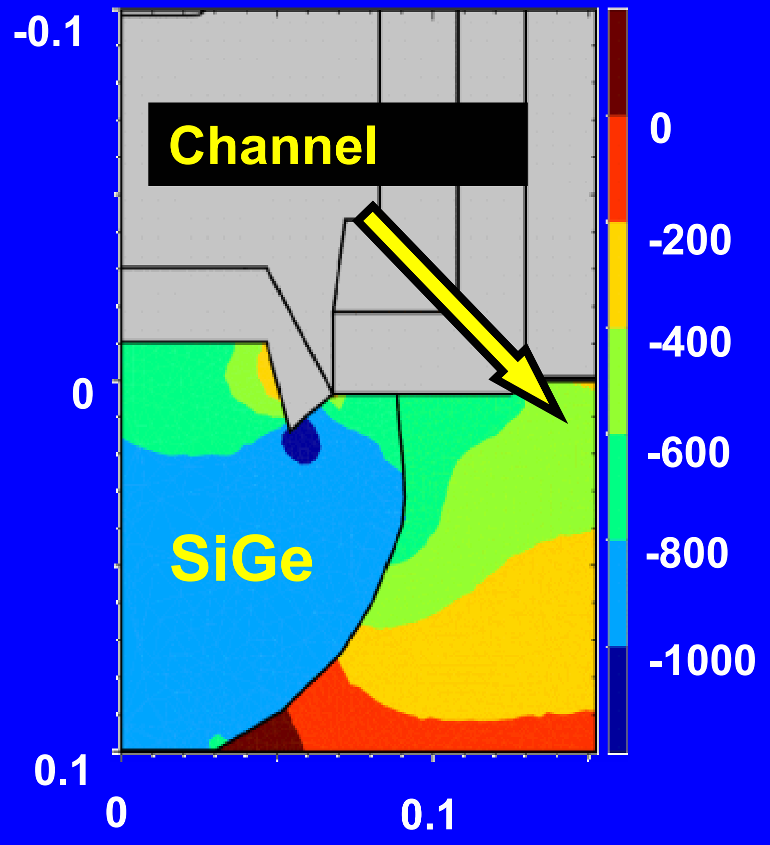
Transistor Results: PMOS

- **Astounding PMOS drive current of 0.72 mA/μm!**
  - at 1.2V and I_{OFF} = 40nA/μm
  - 30% I_{DSAT} gain from strain enhanced mobility

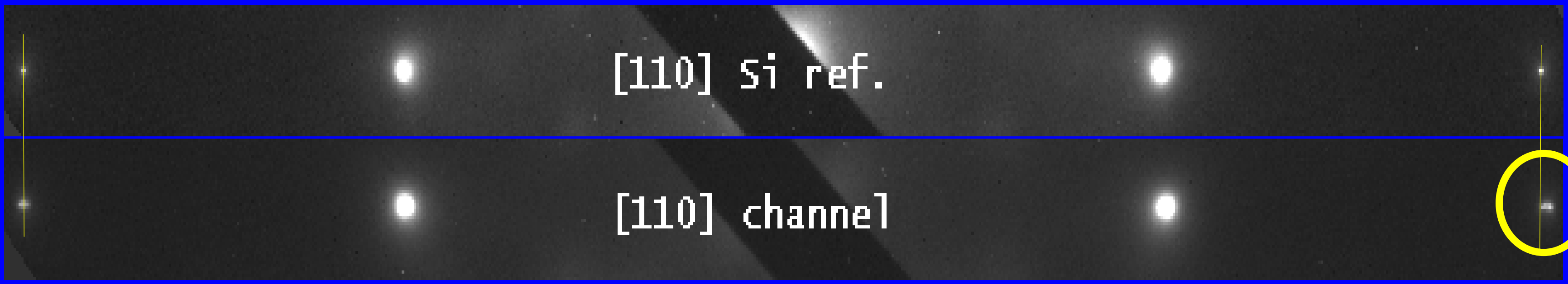


Transistor Results: Channel Strain

- **Simulations show Epitaxial S/D transistor has uniaxial compressive channel strain** [Giles VLSI04]
  - Predicts 55% hole mobility gain
- **TEM electron diffraction measurements confirm 0.6% lattice displacement**

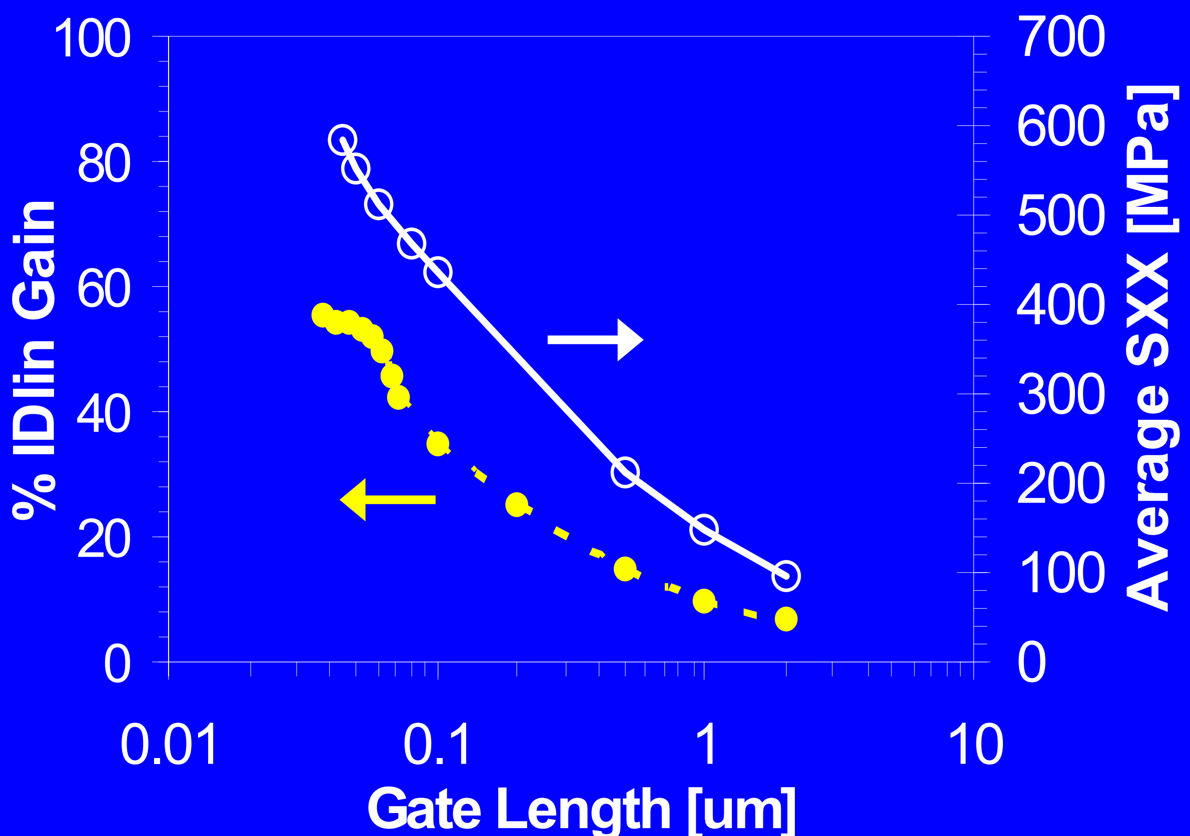


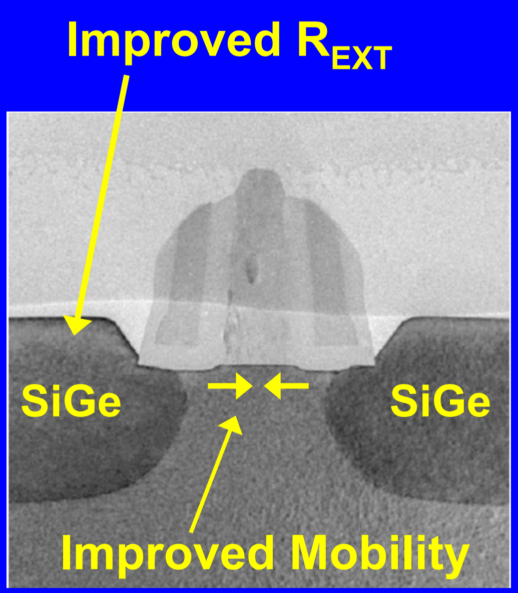
L_{GATE}=50nm



Transistor Results: I_{DLIN} & Strain

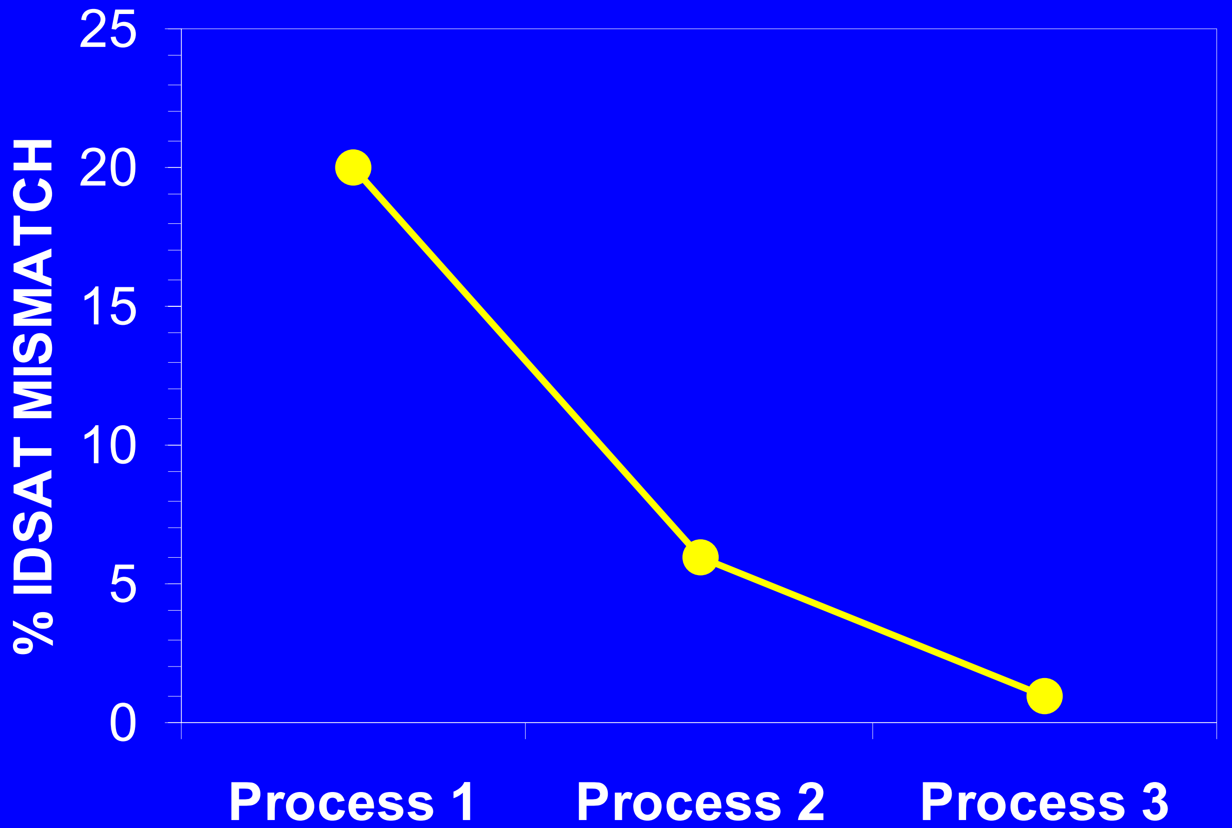
- I_{DLIN} gain vs. L_{GATE} correlated to stress from 2.0μm to 0.1μm
- Both R_{EXT} and strain contribute to gain for < 0.1μm
- Net I_{DLIN} gain of 55% vs. simulated mobility gain of 55%
  - Full mobility gain seen in I_{DLIN}; Epi S/D transistor also improves R_{EXT}





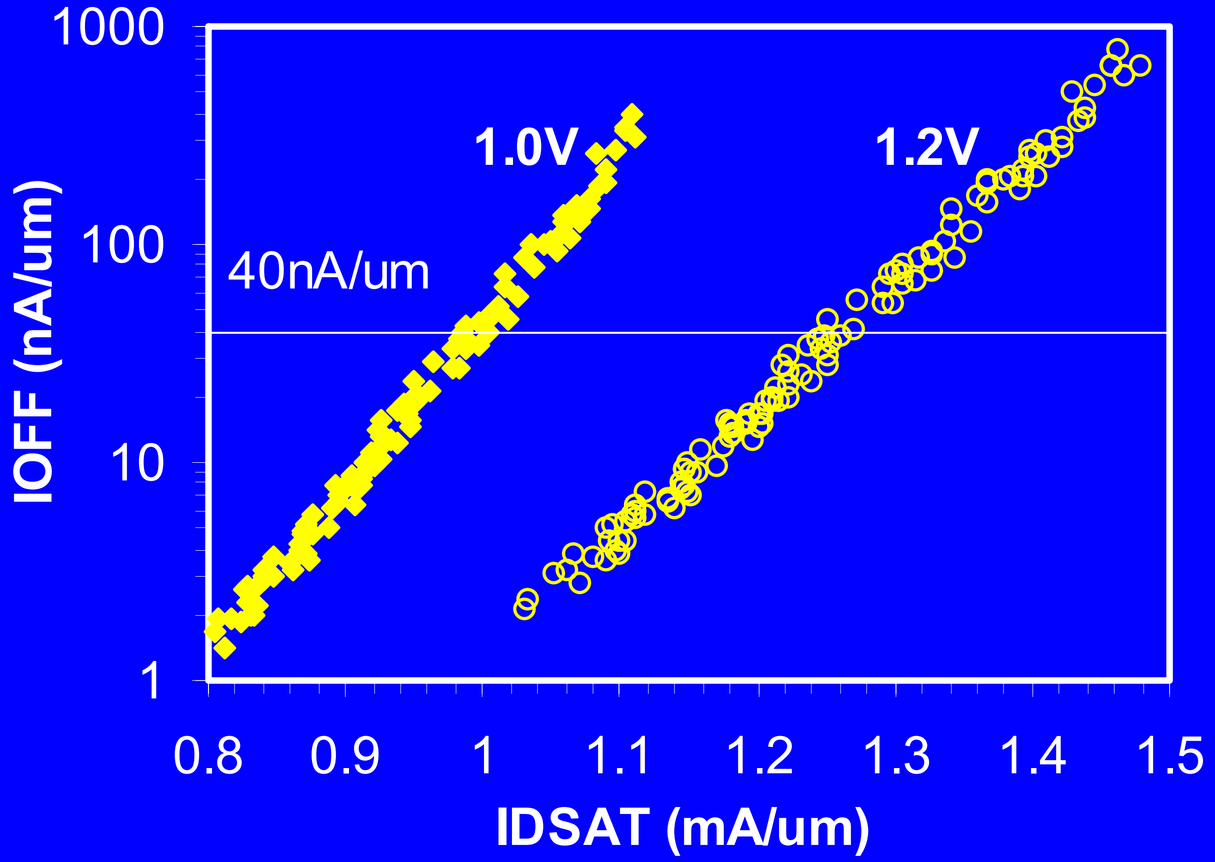
Transistor Results: Pattern Dependence

- PMOS I_{DSAT} for min. poly pitch vs. wider pitch
  - Initial results showed a large difference
  - Minimized with process optimization



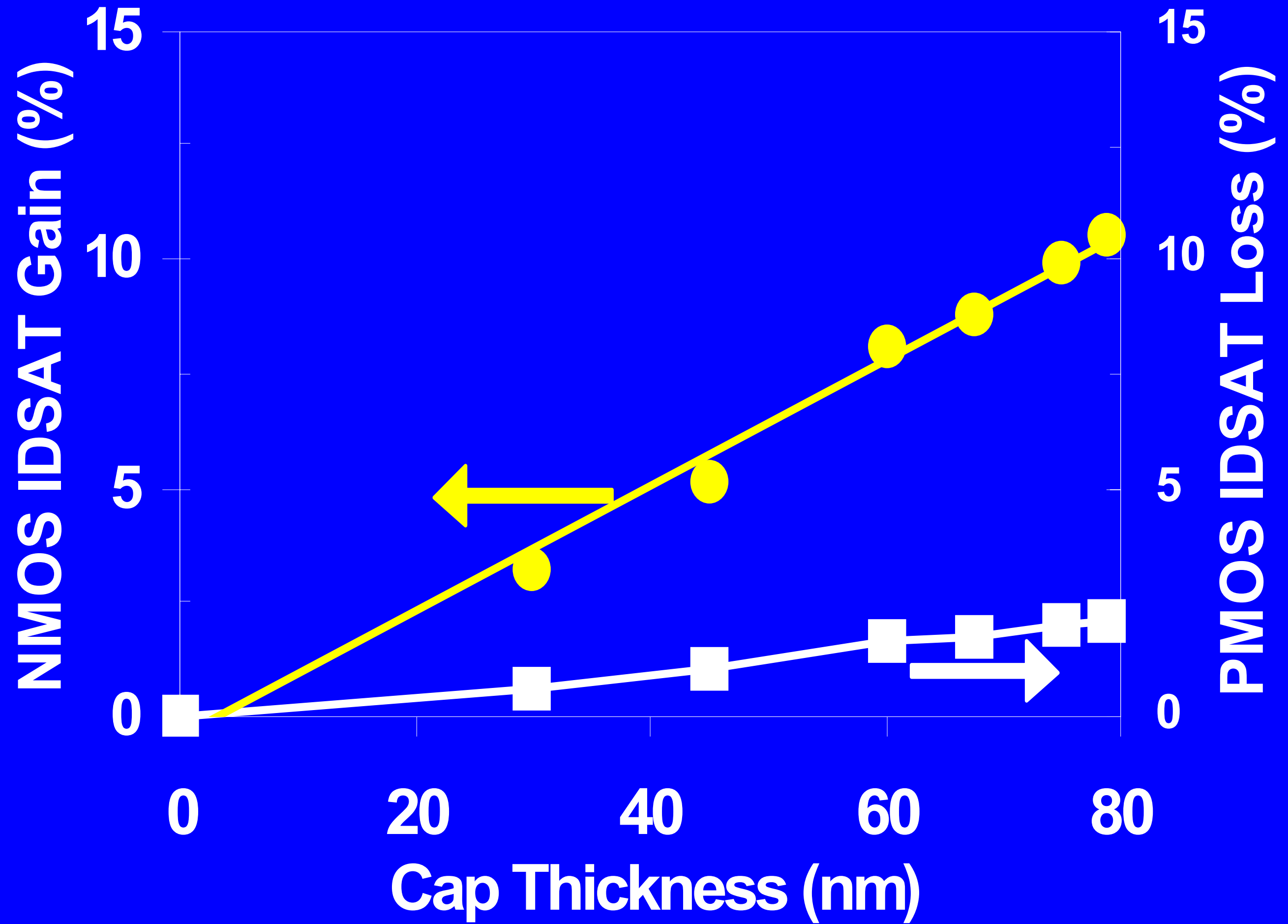
Transistor Results: NMOS

- **Record NMOS drive current of 1.26 mA/um**
  - **10% I_{DSAT} gain from tensile strain layer**



Transistor Results: CMOS

- Tensile capping layer improves NMOS IDSAT with no significant PMOS IDSAT loss



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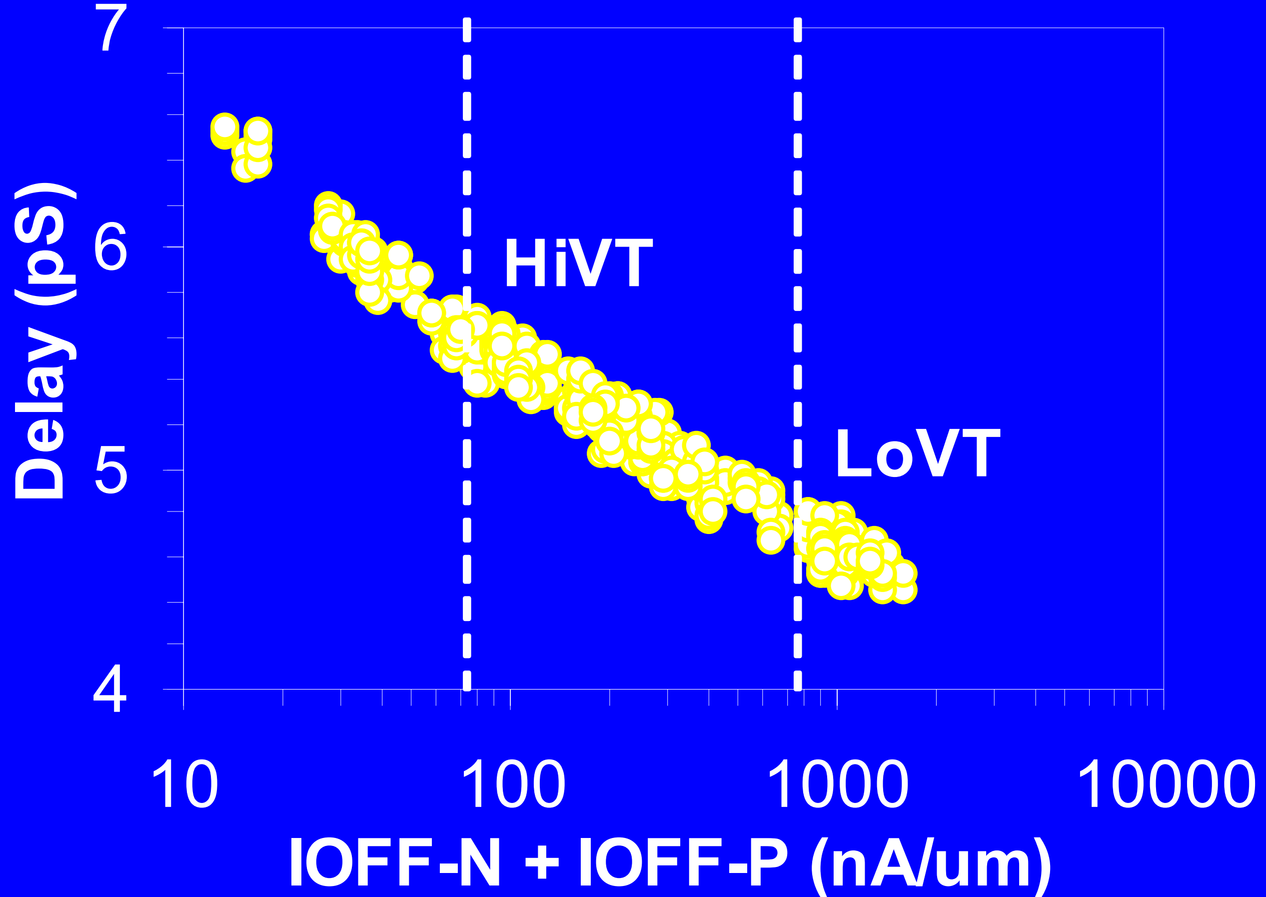
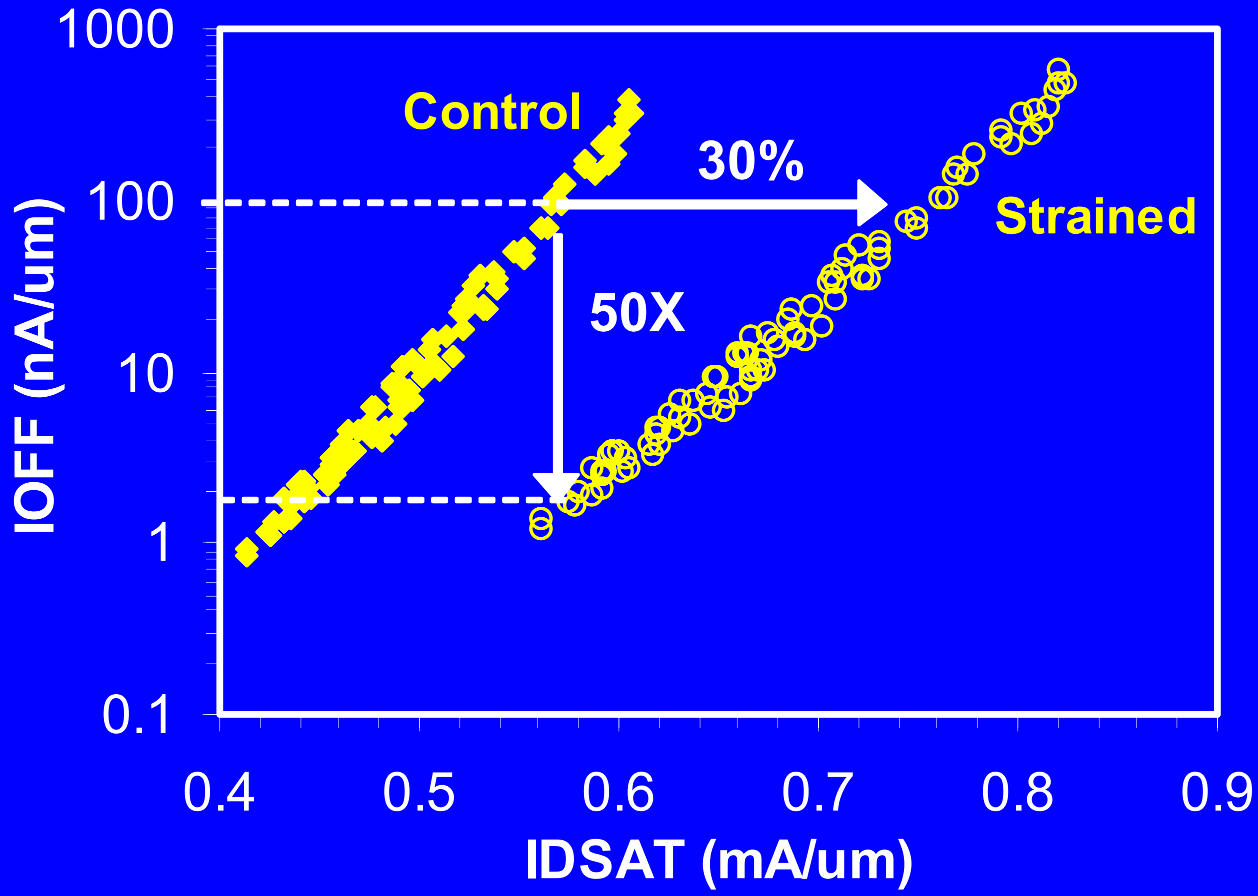
Performance

- Strained silicon results in fast ring oscillators
  - Delay per stage of 4.6pS for low VT devices



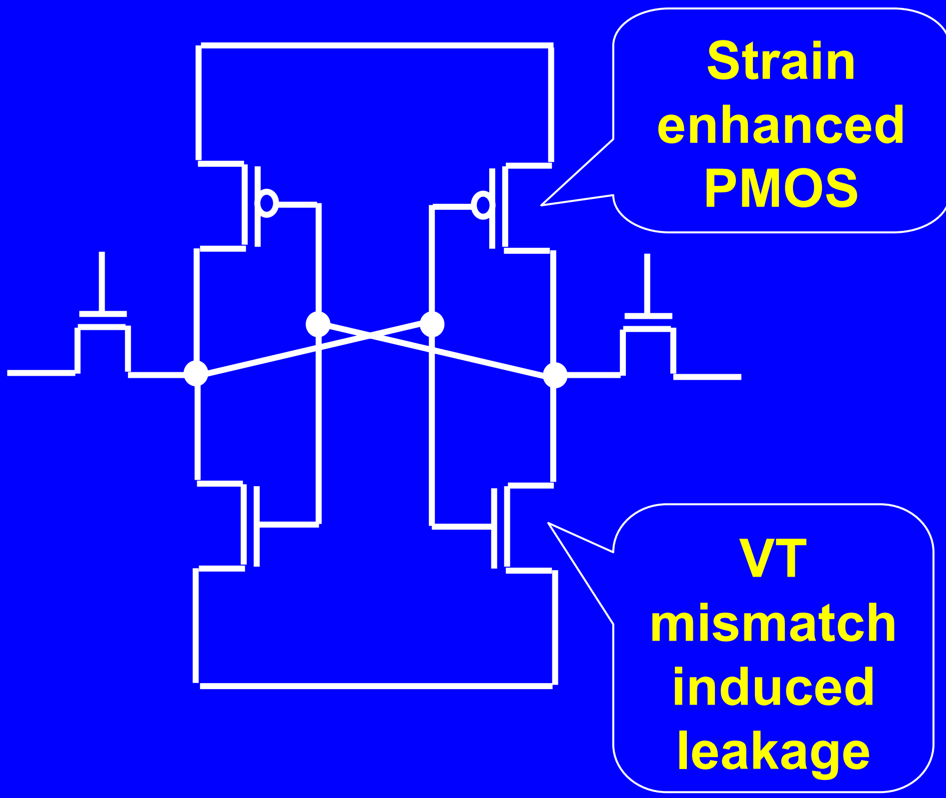
Power: Leakage Reduction

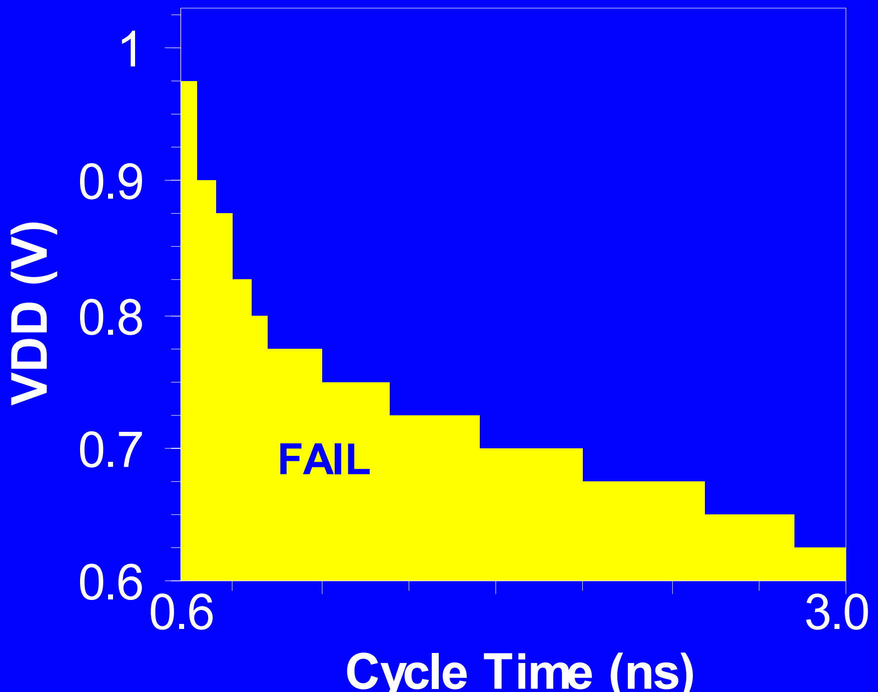
- Strained silicon: high performance, low power
  - Performance: 30% I_{DSAT} gain at fixed I_{OFF}
  - Power: 50X lower I_{OFF} at fixed I_{DSAT}



Power: SRAM VCCmin

- Strain silicon also improves SRAM VCCmin
  - Important for long battery life in mobile applications
  - Strain enhanced PMOS balances V_T mismatch in NMOS
  - 50Mb SRAM with 1.0μm^2 cell functional down to 0.65V





Summary

- Uniaxial strain has significant advantages over biaxial strain for hole mobility enhancement

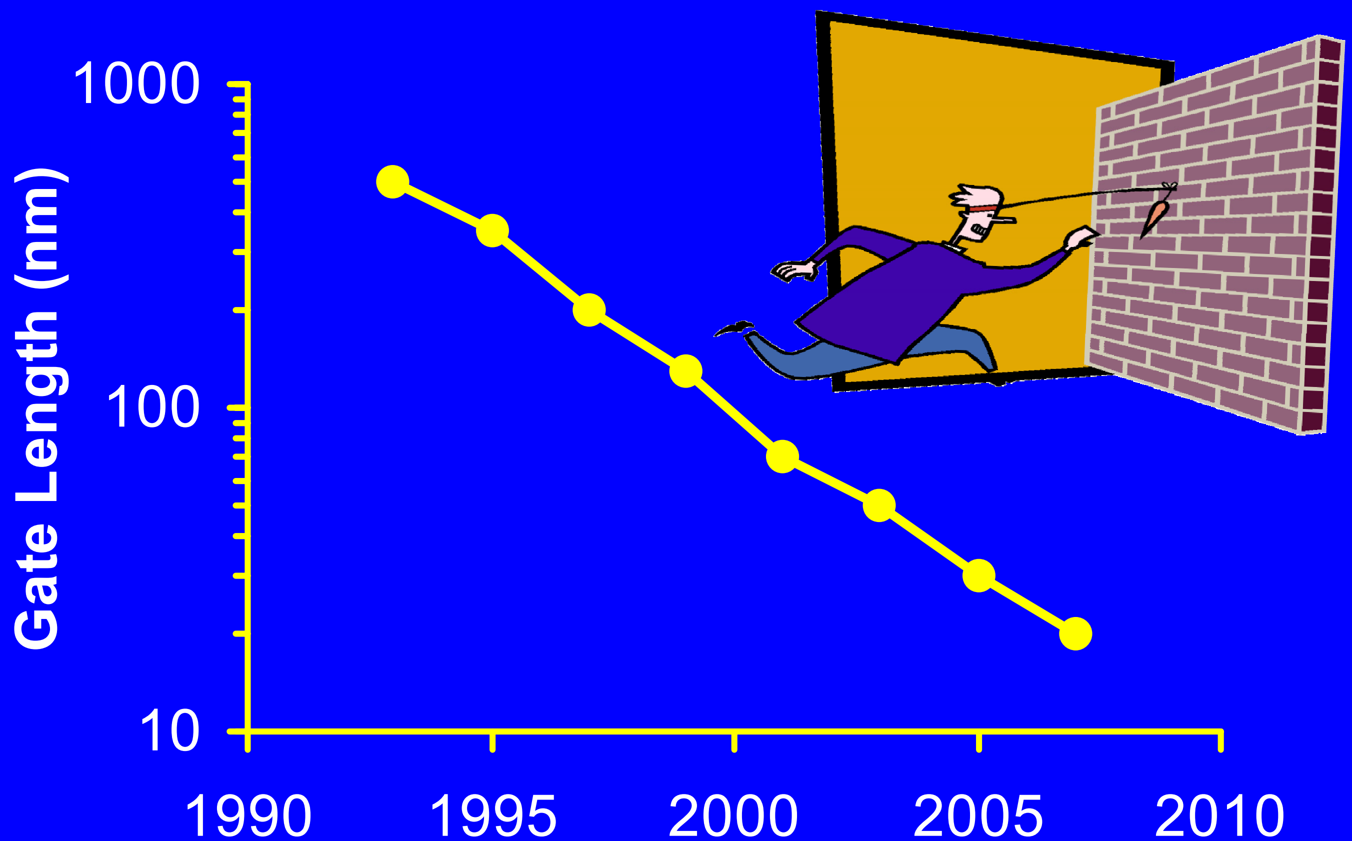
- Epitaxial S/D transistor structure provides
  - Large uniaxial channel strain
  - >50% hole mobility gain and lower R_{EXT}
  - I_{DLIN} sees ALL the mobility gain due to lower R_{EXT}

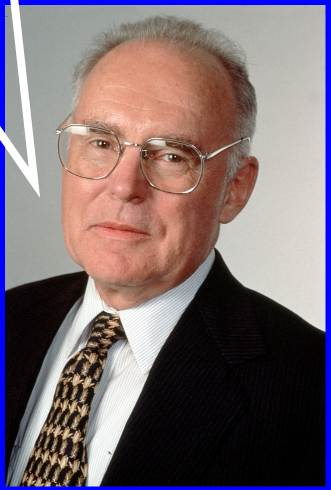
- Strained silicon allows for improved performance and lower power dissipation

Delaying Forever…

- **New materials & structures can extend Moore's law**
  - **Strained silicon is a key example**

No exponential is forever. Your job is to delay forever.





Gordon Moore

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For further information on Intel’s silicon technology

please visit the Silicon Showcase at

www.intel.com/research/silicon